**Amendments to the Claims**

1. (Cancelled) A device comprising:

a package module having a footprint size based on a standard package;

an unpackaged semiconductor die directly attached to the package module; and

a package semiconductor attached to the multi-die module.

2. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor is packaged in a ball grid array package.

3. (Previously Presented) The device as in Claim 56, wherein the unpackaged semiconductor die is a graphics processor.

4. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor is a memory.

5. (Previously Presented) The device as in Claim 56, wherein a plurality of packaged semiconductors are attached to the package module.

6. (Previously Presented) The device as in Claim 56, wherein the unpackaged semiconductor die is wire bonded to the package module.

7. (Withdrawn) The device as in Claim 1, wherein the unpackaged semiconductor die is wire bonded to the package module.

8. (Previously Presented) The device as in Claim 56, wherein attached includes surface-mount technology reflow.

9. (Previously Presented) The device as in Claim 56, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die.

10. (Withdrawn) The device in Claim 1, wherein the unpackaged semiconductor die is underfilled.

11. (Previously Presented) The device as in Claim 56, wherein the footprint size of the package module is one of 35 mm × 35 mm, 31 mm × 31 mm, 27 mm × 27 mm, 37.5 mm × 37.5 mm, 40 mm × 40 mm, 42 mm × 42 mm, or 42.5 mm × 42.5 mm.

12. (Previously Presented) The device as in Claim 56, further including a heat sink.

13. (Previously Presented) The device in Claim 12, wherein a top surface of the unpackaged semiconductor die and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the package module.

14. (Withdrawn) The device as in Claim 12, further including a shim positioned over the unpackaged semiconductor die such that a top of the shim and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the multi-die module.

15. (Cancelled) A device comprising:

a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, and

a packaged memory attached to the package module.

16. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor die is packaged in a ball grid array package.

17. (Previously Presented) The device as in Claim 57, wherein a plurality of packaged memory are attached to the package module.

18. (Previously Presented) The device as in Claim 57, wherein directly attached includes the graphics processing die being wire bonded to the package module.

19. (Withdrawn) The device as in Claim 15, wherein directly attached includes flip-chip attachment.

20. (Previously Presented) The device as in Claim 57, wherein attached includes surface-mount technology reflow.

21. (Cancelled) The device as in Claim 15, wherein the graphics-processing die is encapsulated.

22. (Withdrawn) The device as in Claim 15, wherein the graphics-processing die is underfilled.

23. (Previously Presented) The device as in Claim 57, wherein the standard package sizes include one of 35 mm × 35 mm, 31 mm × 31 mm, 27 mm × 27 mm, 37.5 mm × 37.5 mm, 40 mm × 40 mm, 42 mm × 42 mm, or 42.5 mm × 42.5 mm.

24. (Currently Amended) The device as in Claim [15] 57, further including a heat sink.

25. (Previously Presented) The device in claim 24, wherein a top surface of the graphics-processor die and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

26. (Withdrawn) The device as in Claim 24, further including a shim positioned on top of the graphics-processor die such that a top of the shim and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

27. (Withdrawn) A method comprising the steps of:

directly attaching a first semiconductor die to a package substrate;

forming electrical connections between the first semiconductor die and the package substrate;

securing the electrical connections;

placing a second semiconductor die in a die package;

attaching the die package to the package substrate; and

forming electrical connections between the die package and the package substrate.

28. (Withdrawn) The method as in Claim 27, wherein the step of placing the second semiconductor die in a die package includes placing the semiconductor die in a ball grid array package.

29. (Withdrawn) The method as in Claim 27, wherein the steps of directly attaching and forming electrical connections are performed using a flip-chip process.

30. (Withdrawn) The method as in Claim 27, wherein the steps of attaching and forming electrical connections are performed using surface mount technology reflow.

31. (Withdrawn) The method as in Claim 27, wherein the step of directly attaching includes the use of adhesives.

32. (Withdrawn) The method as in Claim 27, wherein the steps of forming electrical connections include wire-bonding.

33. (Withdrawn) The method as in Claim 27, wherein securing the electrical connections includes encapsulating the first semiconductor die.

34. (Withdrawn) The method as in Claim 27, wherein securing the electrical connections includes underfilling the first semiconductor die.

35. (Withdrawn) The method as in Claim 27, further including the step of attaching solder balls to an underside of the package substrate.

36. (Withdrawn) The method as in Claim 27, wherein the package substrate has a footprint of one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

37. (Withdrawn) The method as in Claim 37, further including the step of attaching a heat sink to the package substrate.

38. (Withdrawn) The method as in Claim 37, further including the step of positioning a shim on top of the first semiconductor die such that a top of the shim and a top surface of the die package are of substantially equal distance from a surface of the package substrate.

39. (Withdrawn) The method as in Claim 27, further including the step of testing the first semiconductor die prior to the step of attaching the die package to the package substrate.

40. (Withdrawn) The method as in Claim 27, further including the step of testing the second semiconductor die after the step of placing the second semiconductor die in a die package and prior to the step of attaching the die package.

41. (Previously Presented) The device as in Claim 9, wherein the encapsulated semiconductor die forms a substantially rectangular structure on the package module.

42. (Previously Presented) The device as in Claim 22, wherein the encapsulated graphics-processing die forms a substantially rectangular structure on the package module.

43. (Cancelled) A multi-die module, comprising:

a substrate having a first surface and a second surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a rectangular footprint; and

a packaged semiconductor die mounted on the first surface of the substrate.

44. (Previously Presented) The multi-die module as in Claim 58, further including a second packaged semiconductor die mounted on the first surface of the substrate.

45. (Previously Presented) The multi-die module as in Claim 58, further including a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

46. (Previously Presented) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is mounted to the first surface of the substrate by wire bonding.

47. (Previously Presented) The multi-die module as in Claim 58, wherein the encapsulating structure is further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

48. (Currently Amended) The multi-die module as in Claim [43] 58, further including a heat sink.

49. (Cancelled) The multi-die module as in Claim 43, wherein each of the unpackaged semiconductor die and packaged semiconductor die has a top surface, and wherein the top surfaces of the unpackaged semiconductor die and the packaged semiconductor die are of substantially equal distance from the first surface of the substrate.

50. (Withdrawn) The multi-die module as in Claim 43, wherein the unpackaged semiconductor die is underfilled.

51. (Withdrawn) The multi-die module as in Claim 43, wherein each of the unpackaged semiconductor die and packaged semiconductor has a top surface, and wherein the distance between top surface of the unpackaged semiconductor die and the first surface of the substrate is different than the distance between the top surface of the packaged semiconductor die and the first surface of the substrate.

52. (Withdrawn) The multi-die module as in Claim 51, further including a shim positioned over the top surface of the packaged semiconductor die such that a top of the shim and the top surface of the packaged semiconductor die are of substantially equal distance from the first surface of the substrate.

53. (Previously Presented) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is a graphics processor.

54. (Previously Presented) The multi-die module as in Claim 58, wherein the packaged semiconductor die is a memory.

55. (Withdrawn) A method of forming a multi-die module, comprising:

mounting a first semiconductor die to a module substrate;

forming an electrical connection between the first semiconductor die and the package module substrate;

encapsulating the first semiconductor die in a rectangular structure;

placing a second semiconductor die in a corresponding die package;

mounting the die package to the module substrate; and

forming an electrical connection between the die package and the module substrate.

56. (Previously Presented) A device comprising:

a package module including a substrate having a standard package footprint;

an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and attached to the package module;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

57. (Previously Presented) A device comprising:

a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a planar top surface; and

a packaged memory die having a top surface and attached to the package module;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

58. (Previously Presented) A multi-die module, comprising:

a substrate having a first surface and a second surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and mounted on the first surface of the substrate;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

59. (Previously Presented) A multi-die module, comprising:

a substrate having a first surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure; and

a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.

60. (Previously Presented) The device of claim 56 further including a planar heat sink adapted to engage the encapsulated structure and the top surface of the packaged semiconductor.